

in Fanout-Free Circuits

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It is shown in a simple manner, a test set for a combinational circuit with n primary input gates and $2n$ primary output gates (and $2n$ primary output gates) nonequivalent single faults over the upper bound in [1, 2] of primary input gates) and of $2n$ for the least number of nonequivalent single faults.

Keywords: single faults, fanout-free circuits, test set.

1. INTRODUCTION

In [1], [2], and [3] we are talking about the standard test set for a combinational circuit. One could consult [1], [2], or [3] if

one wants to know how to detect single faults if given any two faults which means that they differ on n primary input lines in which the two faults differ. It is better than to determine the test set algorithm we present produces a test set of size $n + 1$ where n is the number of primary input lines of the combinational circuit. This is an improvement over [1], [3], and [5].

It is known for fanout-free circuits (see [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41], [42], [43], [44], [45], [46], [47], [48], [49], [50], [51], [52], [53], [54], [55], [56], [57], [58], [59], [60], [61], [62], [63], [64], [65], [66], [67], [68], [69], [70], [71], [72], [73], [74], [75], [76], [77], [78], [79], [80], [81], [82], [83], [84], [85], [86], [87], [88], [89], [90], [91], [92], [93], [94], [95], [96], [97], [98], [99], [100]), we will not bother to discuss the test set algorithm for regular faults. Such a relationship exists and can be worked out by

2. THE ALGORITHM

In this algorithm, we use $T^u(T^z)$ to denote the test set for which the circuit has the value 1(0). The test set T is assumed that we know what the test set looks like on each of the input lines of the circuit. A single fault diagnostic test set is produced for each output gate. Furthermore, to produce the test set algorithm in detail for each output gate G .

Let l_1, \dots, l_k be the input lines of G , and T_1, \dots, T_k be the test sets for the circuits for which l_i is the output line. Note that each $f_i \neq 0, 1$; hence of faults, the output of G

should produce the function $f = f_1 \wedge \dots \wedge f_k \neq 0, 1$. One additional notational convention is that for $t_i \in T_i$ we use (t_1, \dots, t_k) to denote the test that consists of simultaneously applying t_i to the inputs feeding l_i for all i .

With everything as described above, let u_i be an arbitrary member of T_i^z and define

$$\begin{aligned} T^u &= \{(t, u_2, \dots, u_k) \mid t \in T_1^u\} \cup \dots \\ &\quad \cup \{(u_1, \dots, u_{k-1}, t) \mid t \in T_k^u\} \\ T^z &= \{(t, u_2, \dots, u_k) \mid t \in T_1^z\} \cup \dots \\ &\quad \cup \{(u_1, \dots, u_{k-1}, t) \mid t \in T_k^z\} \end{aligned}$$

and

$$T = T^u \cup T^z.$$

Note that T is very close to the set produced by Procedure 2 in [5].

We now have the following theorem.

Theorem: T is a single fault diagnosing test set for the circuit ending at G . $|T^u| = \sum_{i=1}^k |T_i^u| - k + 1$ and $|T^z| = \sum_{i=1}^k |T_i^z| - k + 1$. Thus, $|T| = \sum_{i=1}^k |T_i| - k + 1$.

Proof: If a single fault or no fault occurs in the circuit, then the output of G is one of the functions 0, 1,

$$\begin{aligned} &g_{11} \wedge f_2 \wedge \dots \wedge f_k, \\ &g_{12} \wedge f_2 \wedge \dots \wedge f_k, \dots, g_{1m_1} \wedge f_2 \wedge \dots \wedge f_k, \\ &f_1 \wedge g_{21} \wedge f_3 \wedge \dots \wedge f_k, \dots, f_1 \wedge g_{2m_2} \wedge f_3 \wedge \dots \wedge f_k, \dots, \\ &f_1 \wedge f_2 \wedge \dots \wedge f_{k-1} \wedge g_{km_k}, \quad f_1 \wedge \dots \wedge f_k \end{aligned}$$

where g_{ip} ($p = 1, \dots, m_i$) are the nonequivalent nonzero functions which can occur as a result of a single fault in the circuit having l_i as an output line (see [2], [4]).

Since each $f_1 \wedge \dots \wedge g_{ip} \wedge \dots \wedge f_k$ is 0 on any element of the form $(u_1, \dots, u_{r-1}, t, u_{r+1}, \dots, u_k)$ with $r \neq i$ and $t \in T_r^z$ and 1 on some element of the form $(u_1, \dots, u_{i-1}, t, u_{i+1}, \dots, u_k)$ with $t \in T_i$ (since T_i distinguishes g_{ij} from 0), T clearly distinguishes between 0, 1 and the other faults. Since $T^z \neq \emptyset \neq T^u$, T diagnoses the faults 0, 1.

We now show that if θ, γ are two distinct functions in the list given at the start of the proof such that $\theta, \gamma \neq 0, 1$, then some element of T causes them to assume different values. There are two cases to consider.

Case 1: θ and γ differ only in the i th conjunct. Here it is clear that T distinguishes between θ and γ since some $t \in T_i$ distinguishes between the i th conjunct of θ and γ , whence $(u_1, \dots, u_{i-1}, t, \dots, u_k)$ distinguishes between θ and γ . In particular, this shows that T detects all single faults (it actually detects all multiple faults; see [2], [4]).

Case 2: θ and γ differ in the i th and j th conjuncts with $i \neq j$. Thus, we may assume that $\theta = f_1 \wedge \dots \wedge g_{ip} \wedge f_{i+1} \wedge \dots \wedge f_k$ and $\gamma = f_1 \wedge \dots \wedge g_{jq} \wedge f_{j+1} \wedge \dots \wedge f_k$. Note that θ is 0 on

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$\dots, u_k) | t \in T_i^z$

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Previous sentence is all of T^z ,
between θ and γ or θ and
are done. In the second, we

ally 0 on T^z , then $g_{ip} \equiv 0$
 $f_i, g_{ip} \equiv 0$ on T_i^z and T_i
at l_i , there exist $t_1, t_2 \in T_i^z$
Let $t_1^* = (u_1, \dots, u_{i-1}, t_1,$
 $u_{i+1}, \dots, u_k)$. If $g_{jq}(u_j) = 0,$
 $\theta = 1$, then $\theta(t_1^*) = 0$ while
shes between θ and γ .
m of the $|T_i^z|$ since all the
int, while $|T^z|$ is just the
e the element (u_1, \dots, u_k)
to create T^z . \square

nal circuit with n primary
test set containing exactly

action on n . For $n = 1$ or 2,
the case of the AND gate
ose T_i so that $|T_i| = n_i + 1$
its feeding the line l_i . By the
 $1 = (\sum_{i=1}^k n_i) + 1 = n + 1$.
essentially identical. \square

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ge some stimulating discus-
agnostic test sets and one of

ecture and its relation to fault diag-
Urbana, Rep. R-467, May 1970.
in combinational logic network,"
606, 1971.

quiring a minimal or near-minimal
C-20, pp. 1506-1513, 1971.

e fault test set is smaller than any
national circuit," IBM T. J. Watson
p. RC-6483, Apr. 1977.

ultiple fault diagnosis in fanout free
Tolerant Computing (FTC-5), Paris,